OFFICE INTERFACE UNIT FOR LOOP TIMING (OIU/LT), 628090

GENERAL DESCRIPTION

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1. GENERAL

1.01 This Section provides a general description of the ITT D448 office interface unit for loop timing (OIU/LT), 628090 (Fig. 1), to the functional block diagram level.

1.02 Whenever this Section is reissued, the reasons for reissue will be listed in this paragraph.

1.03 The OIU/LT is an optional unit that loop times the D448 multiplex terminal so the outgoing T1 or TX1C (T1C) clock rate equals the incoming bit rate. One OIU/LT serves two digroups by synchronizing both to a single clock.

2. DESCRIPTION

2.01 The unit mounts in the D448 multiplex shelf (common equipment mounting section) in connector J5C. Installation procedures for the unit are provided in Section ITTR-18-431, ITTR-18-432, or ITTR-18-433.

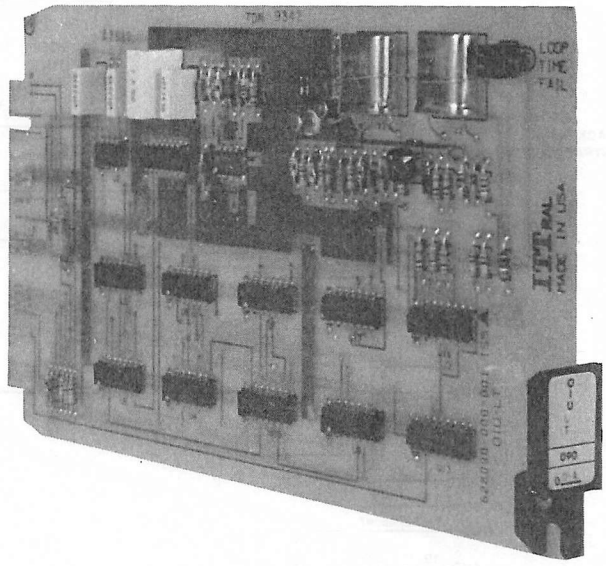

Fig. 1—OIU/LT, 628090

2.02 The unit is available in Group -0 only.

2.03 The unit consists of an epoxy-glass printed circuit board (PCB) and associated circuit components. The lower front edge of the PCB is fitted with a handle to facilitate insertion and removal of the unit from the shelf. An identification strip on the handle face indicates the unit mnemonic (OIU/LT), last three digits of the model number, last three digits of the part number, and issue letter. The part number and issue letter are also located on the component side of the PCB.

2.04 The LOOP TIME FAIL LED (DS1) is located on the front edge of the PCB.

2.05 Printed circuit wiring is etched on both sides of the PCB. The unit inputs and outputs are terminated in gold-plated contacts on the rear edge of the PCB. These contacts mate with a 70-pin contact edge connector on the rear of the multiplex shelf.

3. FUNCTIONAL OPERATION (FIG. 2)

DIGROUP CONTROL

3.01 The digroup control circuit selects the appropriate digroup (A or B) signals, RNDX FR CNT from the

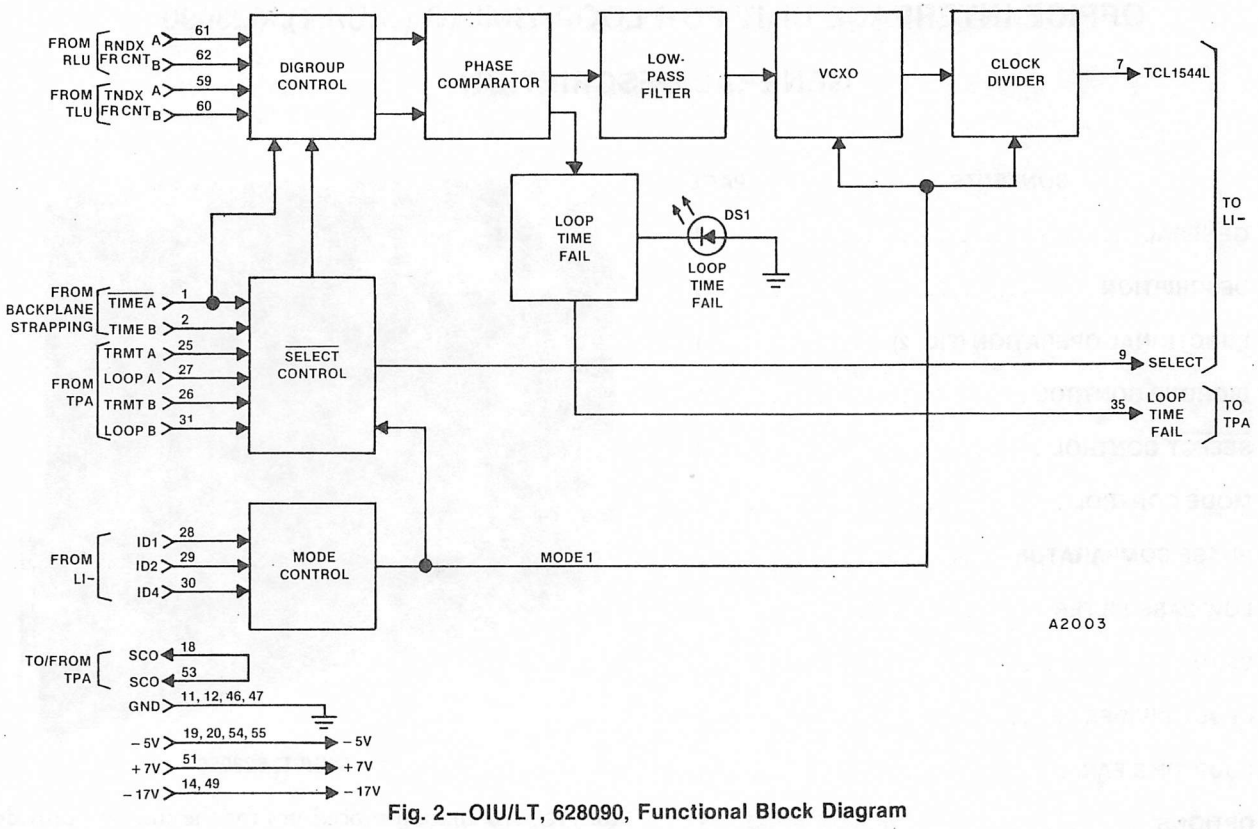

Fig. 2—OIU/LT, 628090, Functional Block Diagram

receive logic unit (RLU) and TNDX FR CNT from the transmit logic unit (TLU), depending upon which timing option [A] or [B]is strapped on the shelf backplane (Section ITTR-18-405 or ITTR-18-406). It forwards the signals to the phase comparator.

SELECT CONTROL

3.02 The select control circuit monitors the digroups via the trunk processor and alarm units (TPAs) for an alarm (TRMT) or a loop (LOOP) condition. If either signal is received, the select control circuit forces the digroup control circuit to select the other digroup. If both digroups are in alarm and/or loop (TRMT and/or LOOP) or no digroup has been selected by backplane strapping, the select control circuit forwards a select signal to the line interface unit (LI-) so the multiplex terminal free runs using the clocks on the LI-s.

MODE CONTROL

3.03 The mode control circuit monitors the mode signals ID1, 2, and 4 from the LI-. When the multiplex terminal is in Mode 1 (ID1), the mode control circuit forces the select control circuit to ignore TRMT B and LOOP B. The mode control circuit also signals the voltage controlled crystal oscillator (VCXO) and clock divider circuits of the appropriate mode.

PHASE COMPARATOR

3.04 The phase comparator circuit receives the appropriate RNDX FR CNT and TNDX FR CNT signals from the digroup control circuit and forwards to the low-pass filter an error signal proportional to the phase difference between the two signals. Also, if the signals are not phase locked, it forwards an out-of-lock signal to the loop time fail circuit.

LOW-PASS FILTER

3.05 The low-pass filter circuit attenuates the high frequency components of the phase comparator circuit output to create a dc error voltage to control the VCXO.

VCXO

3.06 The error voltage generated by the phase comparator and low-pass filter circuits controls the exact frequency of the VCXO so the frequency at the TCL1544L output equals the incoming DS1 or DS1C rate. In Mode 1, the VCXO has a nominal output of 6.304 MHz and in all other modes of 6.176 MHz.

CLOCK DIVIDER

3.07 In Mode 1, the clock divider circuit divides the VCXO output (6.304 MHz) by 2 to provide a

3.152-MHz clock on the TCL1544L output to the LI-. In all other modes, the circuit divides the VCXO output (6.176 MHz) by 4 to provide a 1.544-MHz clock on the TCL1544L output to the LI-.

LOOP TIME FAIL

3.08 If the loop time fail circuit receives an out-of-lock signal from the phase comparator, it causes the LOOP TIME FAIL LED (DS1) to turn on and forwards a loop time fail signal to the TPA.

4. OPTIONS

4.01 This unit has no field-selectable options. However, there are options on the multiplex shelf backplane which affect the operation of this unit. Refer to Section ITTR-18-405 (for shelves mounted in 23-inch bays) or ITTR-18-406 (for shelves mounted in 19-inch bays) for option selection information on these options.

5. SPECIAL FEATURE

5.01 The SCO strap on the backplane connector between pins 18 and 53 must be cut before the unit is inserted. If the OIU/LT is removed from the multiplex shelf while the terminal is in service, a local alarm will occur. The SCO loop on the unit is fed to the TPA unit and if that loop opens, the TPA unit causes a local alarm.

6. TEST AND MAINTENANCE FEATURE

6.01 This unit has LOOP TIME FAIL LED, DS1, which turns on to indicate an out-of-lock condition. Refer to Fig. 1 for the physical location of this feature.

7. TECHNICAL SUMMARY

7.01 A summary of technical specifications for the unit is given in Table A.

TABLE A

ITEM	SPECIFICATION
DC POWER	
Voltage	−5 ±0.25V; −17 ±0.75V; −7 ±0.75V
Current Drain, Maximum	135 mA; 2 mA; 2mA
OPERATING ENVIRONMENT	
Temperature	0° to 55°C
Humidity	To 95% at 40°C (no condensation)
Altitude	To 14,000 ft (4,267 m)

TABLE A (CONT)

ITEM	SPECIFICATION
DIMENSIONS	
Height Width Depth	5.0 in. (12.7 cm) 0.5 in. (1.3 cm) 9.6 in. (24.4 cm)
WEIGHT	0.4 lb (0.2 kg)

8. REPLACEABLE PARTS

8.01 This unit has no field-replaceable parts.

9. REFERENCES

9.01 The engineering drawings noted in Table B were used in the preparation of this Section.

TABLE B

TYPE	DRAWING NO.
Assembly Schematic	628090-000 628090-002

9.02 Related information on the OIU/LT may be found in the ITTR Sections referenced in Table C.

TABLE C

TITLE	SECTION NO.
Connectorized Multiplex Shelf (MS/WC7, MS/WC5, MS/C7 and MS/C6), 628001, 628005, 628011 and 628015 (For 23-Inch Bays) — Option Selection, Installation and Pretest	ITTR-18-405
Connectorized Multiplex Shelf (MS19/WC7, MS19/WC5, MS19/C7 and MS19/C6), 628003, 628008, 628013 and 628018 (For 19-Inch Bays) — Option Selection, Installation and Pretest	ITTR-18-406
Mode 1 Common Equipment — Installation and Pretest	ITTR-18-431
Mode 2 Common Equipment — Installation and Pretest	ITTR-18-432
Mode 3 Common Equipment — Installation and Pretest	ITTR-18-433